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UNITED STATES PATENT APPLICATION

FOR

TWO-STEP GC ETCH FOR GC PROFILE AND PROCESS WINDOW IMPROVEMENT

BY

FANG-YU YEH, CHI LIN AND CHIA-YAO CHEN

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

DESCRIPTION OF THE INVENTION

Field of the Invention

[001] This invention pertains in general to semiconductor fabrication, and, more particularly, to a method of forming gate electrodes in manufacturing semiconductor devices.

Background of the Invention

[002] In recent years, the gate electrode of a metal-oxide-semiconductor field effect transistor ("MOSFET") generally is comprised of a multi-layer structure rather than a single-layer structure. The multi-layer structure may include a polycrystalline silicon layer doped with phosphorus, and a metal silicide layer, for example, a tungsten silicide layer, formed over the polycrystalline silicon layer.

[003] A conventional technique for forming a two-layer gate electrode is shown in Figs. 1A to 1D. Referring to Fig. 1A, a gate oxide layer 12, a polycrystalline silicon layer 14, a tungsten silicide layer 16, and a mask layer 18 are sequentially formed over a semiconductor substrate 10. Mask layer 18 is defined and patterned by a photolithography process. Unmasked portions of tungsten silicide layer 16 and portions of polycrystalline silicon layer 14 underneath the unmasked portions of tungsten silicide layer 16 are sequentially removed by etching processes. The resultant structure is shown in Fig. 1B. In the etching process for tungsten silicide layer 16, tungsten silicide may be removed by low etch selective to polycrystalline silicon. In addition, due to the loading effect, etch rates are different at regions where gate densities are different. Typically, the etch rate at a high-density region, or the array region, is smaller than that of a low-density region, or the

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

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periphery region. As a result, some tungsten silicide may remain at the array region when tungsten silicide at the periphery region is removed.

[004] Referring to Fig. 1C, tungsten silicide layer 16 is over-etched to remove the remaining tungsten silicide at the array region. The over-etch results in non-uniform thickness of polycrystalline silicon layers between the array and periphery regions. However, the thickness control of a polycrystalline silicon layer becomes increasingly important in view of the continued demand for scaled-down device size and high-integration of semiconductor integrated circuits. The non-uniform thickness of polycrystalline silicon layers also may cause failure in an end point detection in an etching process.

[005] Referring to Fig. 1D, the conventional technique then employs a rapid thermal annealing ("RTA") process to anneal tungsten silicide layer 16, and then a rapid thermal oxidation ("RTO") process to form sidewall spacers 20 on tungsten silicide layers 16 and polycrystalline silicon layers 14. However, to ameliorate the non-uniformity defect described above, the thermal stress generated by the RTA followed by the RTO may cause a deformed profile of polycrystalline silicon layer 14, or an over-extrusion of tungsten silicide layer 16, which in turn results in short-circuiting of adjacent contacts.

SUMMARY OF THE INVENTION

[006] Accordingly, the present invention is directed to methods that obviate one or more of the problems due to limitations and disadvantages of the related art.

[007] Additional features and advantages of the invention will be set forth in the description which follows, and in part will be apparent from the description, or

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HENDERSON
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DUNNER LLP

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202.408.4000
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may be learned by practice of the invention. The objectives and other advantages of the invention will be realized and attained by the methods particularly pointed out in the written description and claims thereof, as well as the appended drawings.

[008] To achieve these and other advantages, and in accordance with the purpose of the invention as embodied and broadly described, there is provided a method for manufacturing a semiconductor device that comprises defining a semiconductor substrate, forming a gate oxide on the semiconductor substrate, forming a polycrystalline silicon layer over the gate oxide, forming a tungsten silicide layer over the polycrystalline silicon layer; providing a mask over the tungsten silicide layer, defining the mask to expose at least one portion of the tungsten silicide layer, etching the exposed tungsten silicide layer with a first etchant, wherein some tungsten silicide layer remains, etching the remaining tungsten silicide layer with a second etchant to expose at least one portion of the polycrystalline silicon layer, annealing the tungsten silicide layer, etching the exposed polycrystalline silicon layer, and oxidizing sidewalls of the tungsten silicide layer and the polycrystalline silicon layer.

[009] In one aspect of the present invention, the annealing of the tungsten silicide layer further comprises a rapid thermal annealing process.

[010] In another aspect of the present invention, the oxidizing of sidewalls of the tungsten silicide layer further comprises a rapid thermal oxidization process.

[011] Also in accordance with the present invention, there is provided a method for manufacturing a semiconductor device that comprises defining a semiconductor substrate, forming a gate oxide on the semiconductor substrate,

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HENDERSON
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GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
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forming a polycrystalline silicon layer over the gate oxide, forming a tungsten silicide layer over the polycrystalline silicon layer, providing a mask over the tungsten silicide layer, defining the mask to expose at least one portion of the tungsten silicide layer, etching the exposed tungsten silicide layer with a first etchant, wherein some tungsten silicide layer remains, annealing the tungsten silicide layer, etching the remaining tungsten silicide layer with a second etchant to expose at least one portion of the polycrystalline silicon layer, etching the exposed polycrystalline silicon layer, and oxidizing sidewalls of the tungsten silicide layer and the polycrystalline silicon layer.

[012] Still in accordance with the present invention, there is provided a method of forming a gate structure of a semiconductor device that comprises defining a semiconductor substrate, forming a gate electrode over the semiconductor substrate, the gate electrode comprising a gate oxide, a polycrystalline silicon layer formed over the gate oxide, and a tungsten silicide layer formed over the polycrystalline silicon layer, providing a mask over the gate electrode, defining the mask to expose at least one portion of the tungsten silicide layer, etching the exposed tungsten silicide layer with a first etchant, wherein some tungsten silicide layer remains, etching the remaining tungsten silicide layer with a second etchant to expose at least one portion of the polycrystalline silicon layer, annealing the tungsten silicide layer, etching the exposed polycrystalline silicon layer, and oxidizing sidewalls of the tungsten silicide layer and the polycrystalline silicon layer.

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

[013] Yet still in accordance with the present invention, there is provided a method of forming a gate structure of a semiconductor device that comprises defining a semiconductor substrate, forming a gate electrode over the semiconductor substrate, the gate electrode comprising a gate oxide, a polycrystalline silicon layer formed over the gate oxide, and a tungsten silicide layer formed over the polycrystalline silicon layer, providing a mask over the gate electrode, defining the mask to expose at least one portion of the tungsten silicide layer, etching the exposed tungsten silicide layer with a first etchant, wherein some tungsten silicide layer remains, annealing the tungsten silicide layer, etching the remaining tungsten silicide layer with a second etchant to expose at least one portion of the polycrystalline silicon layer, etching the exposed polycrystalline silicon layer, and oxidizing sidewalls of the tungsten silicide layer and the polycrystalline silicon layer.

[014] It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[015] The accompanying drawings, which are incorporated in and constitute a part of this specification, illustrate embodiments of the invention and, together with the description, serve to explain the objects, advantages, and principles of the invention.

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HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
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202.408.4000
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www.finnegan.com

[016] In the drawings,

[017] Figs. 1A to 1D show a conventional technique in the art for forming a gate electrode of a semiconductor device; and

[018] Figs. 2A to 2F show a method of forming a gate electrode in accordance with one embodiment of the present invention.

DESCRIPTION OF THE EMBODIMENTS

[019] Reference will now be made in detail to the present embodiments of the invention, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers will be used throughout the drawings to refer to the same or like parts.

[020] Figs. 2A to 2F show a method of forming a gate electrode in accordance with one embodiment of the present invention. Referring to Fig. 2A, the method begins with defining a semiconductor substrate 30, which may include cleaning and doping a semiconductor wafer. A gate oxide layer 32, for example, a silicon dioxide (SiO_2) layer, is formed on semiconductor substrate 30. Next, a layered gate structure including a polycrystalline silicon layer 34 and a tungsten silicide layer 36 formed over polycrystalline silicon layer 34 is formed on gate oxide layer 32. A mask layer 38, for example, a silicon nitride layer, is formed over tungsten silicide layer 36. Mask layer 38 is defined and patterned by a conventional photolithography technique.

[021] Fig. 2B is a cross-sectional view of the array region. Fig. 2B' is a cross-sectional view of the periphery region. Referring to Figs. 2B and 2B', unmasked portions of tungsten silicide layer 36 are etched by a first etchant. In one

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

embodiment, the first etchant includes a gas selected from HCl, Cl_2 and He/O_2. Due to the loading effect, when tungsten silicide at the periphery region is removed where gate density is relatively low (Fig. 2B'), some tungsten silicide 36' remains at the array region where gate density is relatively high (Fig. 2B).

[022] Referring to Fig. 2C, an etch back step with a second etchant is performed to remove the remaining tungsten silicide 36'. In one embodiment, the second etchant includes an acid such as NH_4OH/H_2O_2. The etch back process based on the second etchant is performed at a temperature ranging from approximately 55°C to 75°C. With respect to the second etchant, tungsten silicide is etched selectively relative to polycrystalline silicon. The etch-back step reduces sidewalls 36-2 of tungsten silicide layer 36.

[023] Referring to Fig. 2D, a first heat treatment, for example, a rapid thermal annealing ("RTA") process, is performed to anneal tungsten silicide layer 36. The first heat treatment induces a phase transition in tungsten silicide, and increases sidewalls 36-2 of tungsten silicide layer 36 by regrowing tungsten silicide thereon.

[024] Referring to Fig. 2E, unmasked portions of polycrystalline silicon layer 34 are removed by an etching process. Next, referring to Fig. 2F, a second heat treatment, for example, a rapid thermal oxidization ("RTO") process, is performed to form spacers 40 on sidewalls of tungsten silicide layer 36 and polycrystalline silicon layer 34. Since the first and second heat treatments are separated in time from each other by the etching process of polycrystalline silicon layer 34, thermal stress against polycrystalline silicon layer 34 and tungsten silicide layer 36 is alleviated, as compared to the thermal stress generated by the conventional technique.

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

[025] In one embodiment according to the present invention, the step of performing a first heat treatment (Fig. 2D) is conducted before the step of etching the remaining tungsten silicide 36' (Fig. 2C). This embodiment reduces the risk of short-circuiting between adjacent contacts due to over-extrusion of tungsten silicide layer 36.

[026] It will be apparent to those skilled in the art that various modifications and variations can be made in the disclosed methods without departing from the scope or spirit of the invention. Other embodiments of the invention will be apparent to those skilled in the art from consideration of the specification and practice of the invention disclosed herein. It is intended that the specification and examples be considered as exemplary only, with a true scope and spirit of the invention being indicated by the following claims.

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HENDERSON
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GARRETT &
DUNNER LLP

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